CLAIMS

What is claimed is:

1. A method for improving the interfacial strength including adhesion and cohesion between two different layers, said method comprising the steps of:

positioning a substrate having an upper first layer of dielectric or conductive material in a reactor chamber that is capable of generating a plasma;

exposing said upper first layer to a surface preparation plasma for a first period of time;

introducing precursors of a second layer to be deposited on the upper first layer for a second period of time, while the surface preparation plasma is active in the reactor; and

stopping the surface pretreatment plasma at the end of the second period of time and adjusting plasma parameters for deposition of said second layer.

2. The method of Claim 1 wherein the reactor comprises a plasma enhanced chemical vapor deposition reactor, a high-density plasma reactor, a sputtering chamber, or an ion beam chamber.

3. The method of Claim 1 wherein said first layer is a dielectric selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, SiC, SiCH, SiCN, SiCHN, and SiCOH.

4. The method of Claim 1 wherein said second layer is a dielectric that is different from the first layer and is selected from the group consisting of silicon oxide, silicon nitride, silicon oxynitride, SiC, SiCH, SiCN, SiCHN, and SiCOH.

5. The method of Claim 1 wherein said surface preparation plasma comprises a surface pretreatment gas selected from the group consisting of an inert gas, $H_2$, $O_2$, $NH_3$, $SiH_4$ and mixtures thereof.

6. The method of Claim 5 wherein said surface pretreatment gas further comprises F atoms.

7. The method of Claim 1 wherein the substrate is an interconnect structure.

8. The method of Claim 1 wherein said reactor comprises an RF power source for generating said plasmas.

9. The method of Claim 1 wherein the surface preparation plasma comprises Ar gas and said second layer is a dielectric comprising Si, C, O and H.

10. A semiconductor structure comprising:

a substrate having an upper first layer;

a second transition layer located on said upper first layer; and

a third layer located on said second transition layer, wherein said second transition layer provides strong adhesion and cohesive strength between said first and third layers

11. The semiconductor structure of Claim 10 further comprising additional layers atop said third layer, each additional layer is adhered to the underlying layer by a transition layer.

12. The semiconductor structure of Claim 10 wherein said upper first layer is a dielectric material including metal structures embedded therein.

13. The semiconductor structure of Claim 10 wherein said upper first layer is a dielectric material selected from the group consisting of $SiO_2$, TEOS, carbon doped glasses, carbon doped oxides, silicon oxycarbide, SiCOH, SiC, SiCN, SiCH, SiCNH, organic dielectrics and hybrid dielectrics.

14. The semiconductor structure of Claim 10 wherein said third layer is a dielectric layer selected from the group consisting of $SiO_2$, TEOS, carbon doped glasses, carbon doped oxides, silicon oxycarbide, SiCOH, SiC, SiCN, SiCH, SiCNH, organic dielectrics and hybrid dielectrics.

15. An electronic device structure having layers of insulating material functioning as intralevel or interlevel dielectrics comprising:

a semiconductor substrate having a first region of metal embedded in a first layer of insulating material;

a second layer of insulating material including a first region of conductor embedded therein, said second layer of insulating material is separated from said first layer of insulating material by a transition adhesion layer, said first region of conductor is in electrical communication with said first region of metal; and

a third layer of insulating material including a second region of conductor embedded therein, said second region of conductor is in electrical communication with said first region of conductor.

16. The electronic device of Claim 15 further comprising a dielectric cap layer situated between said second layer of insulating material and said third layer of insulating material, said dielectric cap layer being separated from said second layer by a transition layer.

17. The electronic device structure of Claim 16 further comprising an adhesion and cohesion layer of transition between said dielectric cap layer and said third layer of insulating material.

18. The electronic device structure of Claim 15 further comprising: a first dielectric cap layer between said second layer of insulating material and said third layer of insulating material; and a second dielectric cap layer on top of said third layer of insulating material.

19. The electronic device structure of Claim 18 further comprising a transition layer between second dielectric cap layer and said third layer of insulating material.

20. The electronic device structure of Claim 15 further comprising a diffusion barrier layer of a dielectric material deposited on at least one of said second layer of insulating material and said third layer of insulating material.

21. The electronic device structure of Claim 20 further comprising a transition layer between said diffusion barrier layer and said second layer of insulating material and said third layer of insulating material.

22. The electronic device structure of Claim 15 further comprising a dielectric reactive ion etching (RIE) hardmask/polish stop layer on top of said second layer of insulating material, and a dielectric diffusion barrier layer on top of said RIE hardmask/polish stop layer.

23. The electronic device structure of Claim 22 further comprising a transition layer between said dielectric reactive ion etching (RIE) hardmask/polish stop layer and said second layer of insulating material, and a transition layer between said dielectric diffusion barrier layer and said RIE hardmask/polish stop layer.

24. The electronic device structure of Claim 15 further comprising a first dielectric RIE hardmask/polish stop layer on top of said second layer of insulating material;

a first dielectric diffusion barrier layer on top of said first dielectric RIE hardmask/polish stop layer; a second dielectric RIE hardmask/polish stop layer on top of said third layer of insulating material; and a second dielectric diffusion barrier layer on top of said second dielectric RIE hardmask/polish stop layer.

25. The electronic device structure of Claim 24 further comprising transition layers between said first dielectric RIE hardmask/polish stop layer and said first dielectric diffusion barrier layer on top of said first dielectric RIE hardmask/polish stop layer.

26. The electronic device structure of Claim 24 further comprising transition layers between said second dielectric RIE hardmask/polish stop layer and said second dielectric diffusion barrier layer on top of said second dielectric RIE hardmask/polish stop layer.

27. The electronic device structure of Claim 15 further comprising: a dielectric cap layer between an interlevel dielectric of an dielectric material and an intralevel dielectric of an dielectric material.

28. The electronic device structure of Claim 27 further comprising transition layers between said dielectric cap layer and said interlevel dielectric and said intralevel dielectric.